GUJARAT TECHNOLOGICAL UNIVERSITY (GTU)

Competency-focused Outcome-based Green Curriculum-2021 (COGC-2021)
Semester-II

Course Title: Basics of Digital Electronics
(Course Code: 4320703)

Diploma programme in which this course is offered	Semester in which offered
Computer	Second

1. RATIONALE

The engineering technologists (i.e. engineering diploma holders) have to use/maintain various types of equipment which are electronically operated and controlled. For using/maintaining such equipment, the fundamental principles of electronics and electrical are to be applied in many situations to arrive at the probable solutions to many of the broadly defined problems which they will face during their career as technologists. Therefore, the knowledge about the functions of various basic electronics devices and the associated circuits including the associated practical skills acquired through the laboratory will help the student when she/he will be working with electronically controlled/operated equipment or electronic circuits. This course is therefore so designed that the students will be able to apply the principles of digital electronics when required.

2. COMPETENCY

The purpose of this course is to help the student to attain the following industry identified competency through various teaching learning experiences:

- **Use principles of digital electronics in various engineering applications.**

3. COURSE OUTCOMES (COs)

The practical exercises, the underpinning knowledge and the relevant soft skills associated with this competency are to be developed in the student to display the following COs:

a) Perform conversion of given number between various types of number
b) Apply Boolean algebra for circuit optimization
c) Optimize given Boolean expression with K-map
d) Elaborate various types of Combinational circuits
e) Recognize Flip-flops as Sequential **circuits**.

4. TEACHING AND EXAMINATION SCHEME

Teaching Scheme (In Hours)			Total Credits (CI+T/2+P/2)	Examination Scheme				
				Theory Marks		Practical Marks		Total Marks
CI	T	P	C	CA	ESE	CA	ESE	
3	-	2	4	30*	70	25	25	150

(*): Out of 30 marks under the theory CA, 10 marks are for assessment of the micro-project to facilitate integration of COs and the remaining 20 marks is the average of 2 tests to be taken during the semester for the assessing the attainment of the cognitive domain UOs required for the attainment of the COs.

***Legends: CI**-Class Room Instructions; **T** – Tutorial/Teacher Guided Theory Practice; **P** -Practical; **C** – Credit, **CA** - Continuous Assessment; **ESE** -End Semester Examination.*

5. SUGGESTED PRACTICAL EXERCISES

The following practical outcomes (PrOs) that are the sub-components of the COs.*Some of the **PrOs** marked **'*'** are compulsory, as they are crucial for that particular CO. These PrOs need to be attained at least at the 'Precision Level' of Dave's Taxonomy related to 'Psychomotor Domain'*.

S. No.	Practical Outcomes (PrOs)	Unit No.	Approx. Hrs. required
1	Convert Number system to another (Binary, Decimal, Octal, Hexadecimal)	I	06
2	Calculate R's and (R-1)'s Complements	I	02
3	Implement the basic logic gates.	II	02
4	Implement the NAND gate as a universal building block.	II	02
5	Implement the NOR gate as a universal building block.	II	02
6	Simplify and design Boolean expression using basic logic gates	II	02
7	Simplify and design Boolean expression using Universal gates	III	02
8	Design and implement Half Adder and full adder circuit.	IV	02
9	Design and implement Half Subtractor and full Subtractor circuit.	IV	02
10	Realize Multiplexer and Demultipxer circuit	IV	02
11	Realize Decoder and Encoder circuit	IV	02
12	Implement various types of flip-flops	V	02
	Total		**28**

Note

i. *More **Practical Exercises** can be designed and offered by the respective course teacher to develop the industry relevant skills/outcomes to match the COs. The above table is only a suggestive list.*

ii. *The following are some **sample** 'Process' and 'Product' related skills (more may be added/deleted depending on the course) that occur in the above listed **Practical Exercises** of this course required which are embedded in the COs and ultimately the competency..*

S. No.	Sample Performance Indicators for the PrOs	Weightage in %
1	Prepare of experimental setup	20
2	Operate the equipment setup or circuit	20
3	Follow safe practices measures	10
4	Record observations correctly	20
5	Interpret the result and conclude	30
Total		**100**

6. MAJOR EQUIPMENT/ INSTRUMENTS AND SOFTWARE REQUIRED

These major equipment/instruments and Software required to develop PrOs are given below with broad specifications to facilitate procurement of them by the

administrators/management of the institutes. This will ensure conduction of practical in all institutions across the state in proper way so that the desired skills are developed in students.

S. No.	Equipment Name with Broad Specifications	PrO. No.
1	Logic gates Digital Electronics Trainer kit	All
2	Variable DC power supply 0- 30V, 2A, SC protection, display for voltage and current.	All
3	Digital Multimeter : 3 1/2 digit display, 9999 counts digital multimeter measures: V_{ac}, V_{dc} (1000V max) , A_{dc}, A_{ac} (10 amp max) , Resistance (0 - 100 MΛ) , Capacitance and Temperature measurement	All
4	Electronic Work Bench : Bread Board 840 -1000 contact points : Positive and Negative power rails on opposite side of the board , 0-30 V , 2 Amp Variable DC power supply, Function Generator 0-2MHz, CRO 0-30MHz , Digital Multimeter.	All

7. AFFECTIVE DOMAIN OUTCOMES

The following ***sample*** Affective Domain Outcomes (ADOs) are embedded in many of the above mentioned COs and PrOs. More could be added to fulfil the development of this competency.

a) Work as a leader/a team member.
b) Follow ethical practices.

The ADOs are best developed through the laboratory/field based exercises. Moreover, the level of achievement of the ADOs according to Krathwohl's 'Affective Domain Taxonomy' should gradually increase as planned below:

i. 'Valuing Level' in 1st year
ii. 'Organization Level' in 2nd year.
iii. 'Characterization Level' in 3rd year.

9. UNDERPINNING THEORY

The major Underpinning Theory is formulated as given below and only higher level UOs of *Revised Bloom's taxonomy* are mentioned for development of the COs and competency in the students by the teachers. (Higher level UOs automatically include lower level UOs in them). If required, more such higher level UOs could be included by the course teacher to focus on attainment of COs and competency.

Unit	Unit Outcomes (UOs) (4 to 6 UOs at Application level)	Topics and Sub-topics
Unit-I Binary Systems	1.1 Demonstrate Number systems and binary codes 1.2 Convert Number systems and its complements 1.3 Binary codes	● Introduction of Digital Systems ● Binary numbers ● Base Conversion -Binary -Decimal -Octal -Hexadecimal

		● Complements •R's Complement •(R-1)'s Complement •2' and 10's Complement •1's and 9's Complement ● Binary Codes -Weighted Codes -Non weighed codes -Gray Code -Excess-3 Code
Unit – II Binary Logic And Boolean Algebra	1.1 Explain Binary Logic 2.2 List and explain working of Logic Gates 2.3 Interpret Boolean postulates, laws and theorams 2.4. Simplify Boolean expression	● Binary logic ● Logic Gates AND , OR, NOT, EX-OR, NOR, NAND, EX-NOR ● Universal Gates -NAND Gate -NOR Gate ● Postulates ● Laws ● Boolean algebra ● De-Morgan's Theorems ● Boolean functions
Unit – III Boolean Function Implement ation	1.1 Explain Boolean function Simplification using Karnaugh map 1.2 Implementation of Boolean functions 1.3 Identify universal gates	● Need for simplification ● Simplification by Karnaugh map(K-map) method -2 – Variable K – map -3 – Variable K – map -4 – variable K – map ● K – Map using Don't care condition ● NAND Implementation ● NOR Implementation
Unit– IV Basic Combinatioa nal circuits	4.1 Explain Basic Combinational circuits 4.2 Arithmatic and Logical Combinational Circuits 4.3 Data transmission combinational circuits.	● Introduction to combinational circuits ● Arithmatic and Logical Combinational Circuits -Half Adder -Full Adder -Half Subtractor -Full Subtractor ● Data transmission combinational circuits. Encoder -4 – 2 Encoder Decoder -2 – 4 Decoder

		Multiplexer -4 – 1 multiplexer Demultiplexer -1 – 4 Demultiplexer
Unit– V Basic Sequential circuits	5.1 Explain Basic Sequential circuits 5.2 Flip-flops	● Introduction to sequential circuits ● Flip-flops -SR Flip flop -JK Flip flop -D Flip flop -T Flip flop

***Note**: The UOs need to be formulated at the 'Application Level' and above of Revised Bloom's Taxonomy' to accelerate the attainment of the COs and the competency.*

10. SUGGESTED SPECIFICATION TABLE FOR QUESTION PAPER DESIGN

Unit No.	Unit Title	Teaching Hours	Distribution of Theory Marks			
			R Level	U Level	A Level	Total Marks
I	Binary System	10	4	7	7	18
II	Binary Logic and Boolean Alegebra	12	5	7	8	20
III	Boolean Function Implementation	08	4	4	6	14
IV	Basics of Combinational Circuit	08	2	5	5	12
V	Basics of Sequential Circuit	04	1	2	3	6
Total		**42**	**16**	**25**	**29**	**70**

Legends: *R=Remember, U=Understand, A=Apply and above (Revised Bloom's taxonomy)*
Note*: This specification table provides general guidelines to assist students for their learning and to teachers to teach and question paper designers/setters to formulate test items/questions assess the attainment of the UOs. The actual distribution of marks at different taxonomy levels (of R, U and A) in the question paper may vary from above table.*

11. SUGGESTED STUDENT ACTIVITIES

Other than the classroom and laboratory learning, following are the suggested student-related ***co-curricular*** activities which can be undertaken to accelerate the attainment of the various outcomes in this course: Students should conduct following activities in groups and prepare small reports (of 1 to 5 pages for each activity). For micro project reports should be as per suggested format, for other activities students and teachers together can decide the format of the report. Students should also collect/record physical evidences such as photographs/videos of the activities for their (student's) portfolio which will be useful for their placement interviews:

a) Prepare specifications of some electronic devices.
b) Undertake micro-projects in groups(Max. Limit-4)
c) Give seminars on any relevant topic.
d) Prepare showcase portfolios.

12. SUGGESTED SPECIAL INSTRUCTIONAL STRATEGIES (if any)

These are sample strategies, which the teacher can use to accelerate the attainment of the various outcomes in this course:

a) Massive open online courses (***MOOCs***) may be used to teach various topics/subtopics.
b) Guide student(s) in undertaking micro-projects.
c) ***'CI" in section No. 4***means different types of teaching methods that are to be employed by teachers to develop the outcomes.
d) About ***20% of the topics/sub-topics*** which are relatively simpler or descriptive in nature is to be given to the students for ***self-learning***, but to be assessed using different assessment methods.
e) With respect to ***section No.11***, teachers need to ensure to create opportunities and provisions for ***co-curricular activities***.
f) Guide students for using data manuals.

13. SUGGESTED MICRO-PROJECTS

Only one micro-project is planned to be undertaken by a student that needs to be assigned to him/her in the beginning of the semester. In the first four semesters, the micro-project are group-based (group of 3 to 5). However, **in the fifth and sixth semesters**, the number of students in the group should ***not exceed four.***

The micro-project could be industry application based, internet-based, workshop-based, laboratory-based or field-based. Each micro-project should encompass two or more COs which are in fact, an integration of PrOs, UOs and ADOs. Each student will have to maintain a dated work diary consisting of individual contributions in the project work and give a seminar presentation of it before submission. The total work load on each student due to the micro-project should be about ***16 (sixteen) student engagement hours*** (i.e. about one hour per week) during the course. The students ought to submit micro-project by the end of the semester (so that they develop the industry oriented COs).

A suggestive list of micro-projects is given here. This should relate highly with competency of the course and the COs. Similar micro-projects could be added by the concerned course teacher:

a) Build the circuits for implementing AND gates using NAND gates.
b) Build the circuits for implementing OR gates using NAND gates.
c) Build the circuits for implementing AND gates using NOR gates.
d) Build the circuits for implementing OR gates using NOR gates**.**

14. SUGGESTED LEARNING RESOURCES

S. No.	Title of Book	Author	Publication with place, year and ISBN
1	Digital logic and Computer Design	Mano M Morris	Pearson publication Latest Edition ISBN:81-203-0417-9
2	Morden Digital Electronics	Jain R P	Tata Macgrowhill Latest Edition
3	Digital Electronic Principals	Malvino and Litch	Tata Macgrowhill Latest Edition
4	Fundamentals of Digital Circuits	Anand kumar	Prentice-hall of India Latest Edition

15. SUGGESTED LEARNING WEBSITES

a) www.datasheetcafe.com
b) www.williamson-labs.com
c) www.learnerstv.com
d) www.cadsoft.io
e) www.nptel.iitm.ac.in
f) www.khanacademy
g) www.vlab.co.in
h) www.asic-world.com/digital/tutorial.html

16. PO-COMPETENCY-CO MAPPING

Semester II	Basics of Digital Electronics (Course Code: .....)								
	POs and PSOs								
Competency & Course Outcomes	PO 1 Basic & Discipline specific knowledge	PO 2 Problem Analysis	PO 3 Design/development of solutions	PO 4 Engineering Tools, Experimentation &Testing	PO 5 Engineering practices for society, sustainability & environment	PO 6 Project Management	PO 7 Life-long learning	PSO 1	PSO 2
Competency *Use principles of basic electronics in various engineering applications*									
Course Outcomes *CO1 Perform conversion of given number between various types of number*	2	1	1	-	-	-	1		
CO2 Apply Boolean algebra for circuit optimization	2	1	1	-	-	-	1		
CO3 Optimize given Boolean expression with K-map	2	1	1	-	-	-	-		
CO4 Elaborate various types of Combinational circuits	2	-	-	-	-	-	-		
CO5 Recognize Flip-flops as Sequential circuit.	2	-	-	-	-	-	-		

Legend: '**3**' for high, '**2**' for medium, **'1'** for low or **'-'** for the relevant correlation of each competency, CO, with PO/ PSO

15. COURSE CURRICULUM DEVELOPMENT COMMITTEE

GTU Resource Persons

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