GUJARAT TECHNOLOGICAL UNIVERSITY (GTU)

Competency-focused Outcome-based Green Curriculum-2021 (COGC-2021)
Semester-II

Course Title: Digital Electronics
(Course Code: 4321102)

Diploma programme in which this course is offered	Semester in which offered
Electronics & Communication Engineering	Second

1. RATIONALE

Digital technology is the fastest growing technology and have revolutionized the electronics Industry. In most of the applications digital technology has replaced analogue technology. Digital logic is heart of digital electronic circuits. A basic understanding of this subject is therefore essential to effectively maintain digital electronic devices. The study of this course will enable the students to test the working and rectify the faults of common digital circuits.

2. COMPETENCY

The course content should be taught and implemented with the aim to develop different types of skills so that students are able to acquire following competency:

- **Maintain the digital electronic circuits.**

3. COURSE OUTCOMES (COs)

The practical exercises, the underpinning knowledge and the relevant soft skills associated with the identified competency are to be developed in the student for the achievement of the following COs:

a) Interpret various number systems and their conversions with binary arithmetic operations.
b) Implement simplified Boolean equations using logic gates.
c) Test different types of combinational logic circuits.
d) Test different types of sequential logic circuits.
e) Classify various memories and logic families.

4. TEACHING AND EXAMINATION SCHEME

Teaching Scheme (In Hours)			Total Credits (L+T+P/2)	Examination Scheme				
				Theory Marks		Practical Marks		Total Marks
L	T	P	C	CA	ESE	CA	ESE	
3	0	2	4	30*	70	25	25	150

(*): Out of 30 marks under the theory CA, 10 marks are for assessment of the micro-project to facilitate integration of COs and the remaining 20 marks is the average of 2 tests to be

taken during the semester for the assessing the attainment of the cognitive domain UOs required for the attainment of the COs.

***Legends: L**-Lecture; **T** – Tutorial/Teacher Guided Theory Practice; **P** -Practical; **C** – Credit, **CA** - Continuous Assessment; **ESE** -End Semester Examination.*

5. SUGGESTED PRACTICAL EXERCISES

Following practical outcomes (PrOs) are the sub-components of the Course Outcomes (Cos). Some of the **PrOs** marked **'*'** are compulsory, as they are crucial for that particular CO at the 'Precision Level' of Dave's Taxonomy related to 'Psychomotor Domain'.

Sr. No.	Practical Outcomes (PrOs)	Unit No.	Approx. Hrs. Required
1	Build/Test the functionality of Basic and Advance Logic Gates**.**	2	02*
2	Build/Test 2 input basic logic gates using NAND gate.	2	02*
3	Build/Test 2 input basic logic gates using NOR gate.	2	02*
4	Build/Test logic circuits for De Morgan's theorems.	2	02*
5	Build/Test Half Adder Circuit.	3	02*
6	Build/Test Full Adder Circuit using two half adders.	3	02*
7	Build/Test Full Subtractor Circuit.	3	02
8	Build/Test the Decoder/ Demultiplexer circuit.	3	02*
9	Build/Test the Multiplexer circuit.	3	02
10	Build/Test a circuit to Convert 4 bit Binary to Gray Code using logic gates.	1,3	02*
11	Build/Test a circuit to Convert 4 bit Gray to Binary Code using logic gates.	1,3	02
12	Build/Test the functionality of the SR and D Flip-Flop.	4	02*
13	Build/Test the functionality of the JK and T Flip-flops.	4	02*
14	Build/Test the working of the Shift Register/Ring counter.	4	02
15	Build/Test the working of BCD Counter.	4	02*
16	Identify various semiconductor memories (RAM, ROM) from CPU and list their features/specifications.	5	02
17	Identify various Digital Logic families and prepare characteristics comparison.	5	02*
	Minimum 12 Practical Exercises		**24**

Note

*i. More **Practical Exercises** can be designed and offered by the respective course teacher to develop the industry relevant skills/outcomes to match the COs. The above table is only a suggestive list.*

ii. Care must be taken in assigning and assessing study report as it is a first year study report. Study report, data collection and analysis report must be assigned in a group. Teacher has to discuss about type of data (which and why) before group start their market survey.

The following are some **sample** 'Process' and 'Product' related skills (more may be added/deleted depending on the course) that occur in the above listed **Practical Exercises** of this course required which are embedded in the COs and ultimately the competency.

S. No.	Sample Performance Indicators for the PrOs	Weightage in %
1	Prepare of experimental setup	20
2	Operate the equipment setup or circuit	20
3	Follow safe practices measures	10
4	Record observations correctly	20
5	Interpret the result and conclude	30
Total		**100**

6. MAJOR EQUIPMENTS/ INSTRUMENTS REQUIRED

These major equipments with broad specifications for the PrOs is a guide to procure them by the administrators to user in uniformity of practical's in all institutions across the state.

Sr. No.	Equipment Name with Broad Specifications	PrO. No.
1.	Digital IC Trainer Kit	1,2,3,4,5,6,7
2.	Digital Logic Gate ICs (74XX)	1,2,3,4,5,6,7
3.	• Digital Multimeters: Vac, Vdc (1000V max), I_{dc}, I_{ac} (10 amp max), Resistance (0 - 100 MW) , Capacitance. • Breadboards	1,2,3,4,5,6,7
4.	• Cathode Ray Oscilloscope (20MHz Dual Channel) • Function Generator	1,2,3,4,5,6,7
5.	Verification of NAND and NOR gate as universal gate Trainer Kit	2,3
6.	Digital IC Tester	1,2,3,4,5,6,7
7.	Decoder/demultiplexer Trainer Kit	8
8.	Encoder/Multiplexer Trainer Kit	9
9.	Code Converter Trainer Kit	10,11
10.	RS/D/JK flip flop Trainer Kit	12,13
11.	Digital Counter Trainer Kit	14,15
12.	Different types of Semiconductor Memories (RAM and ROM)	16

7. AFFECTIVE DOMAIN OUTCOMES

The following ***sample*** Affective Domain Outcomes (ADOs) are embedded in many of the above-mentioned COs and PrOs. More could be added to fulfill the development of this course competency.

a) Work as a leader/a team member.
b) Follow ethical practices.
c) Follow safety precautions.
d) Realize importance of E-waste management.

The ADOs are best developed through the laboratory/field based exercises. Moreover, the level of achievement of the ADOs according to Krathwohl's 'Affective Domain Taxonomy' should gradually increase as planned below:

i. 'Valuing Level' in 1st year
ii. 'Organization Level' in 2nd year.
iii. 'Characterization Level' in 3rd year.

8. UNDERPINNING THEORY

The major underpinning theory is given below based on the higher level UOs of *Revised Bloom's taxonomy* that are formulated for development of the COs and competency. If required, more such UOs could be included by the course teacher to focus on attainment of COs and competency.

Unit	Unit Outcomes (UOs) (4 to 6 UOs at different levels)	Topics and Sub-topics
Unit-I **Number systems and codes**	1a. Interpret various number systems 1b. Convert a number from one numbering system to another 1c. Perform arithmetic operations on Binary numbers 1d. Interpret the Binary codes.	1.1 Introduction to different Number Systems: Binary, Octal, Decimal, Hexadecimal 1.2 Conversion from One Number system to another 1.3 Binary arithmetic operations: 1.3.1 addition, subtraction, multiplication and division 1.3.2 1's and 2's Complement & Subtraction using complement method 1.4 Codes: BCD, Gray, ASCII
Unit– II **Boolean algebra and logic gates**	2a. Describe functions of logic gates 2b. Explain logic operations, theorems and properties of Boolean algebra 2c. Explain Boolean functions and implement using logic gates 2d. Simplify the Boolean function	2.1 Digital Logic Gates: Symbol, operation and truth-table of AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR gates. 2.2 Basic theorems and properties of Boolean algebra. 2.3 AND-OR -Invert implementations of Boolean function 2.4 Universal Gates: NAND & NOR 2.5 Algebraic simplification of Boolean expression 2.6 Sum of Product (SOP) Simplification using Karnaugh map (K-map) upto 4-variables

Unit	Unit Outcomes (UOs) (4 to 6 UOs at different levels)	Topics and Sub-topics
		2.7 Don't care condition in K-map
Unit-III **Combinational logic circuits**	3a. Explain function of combinational circuits 3b. Implement various combinational circuits. 3c. Implement code converter circuit.	3.1 Arithmetic Circuits: Half adder, full adder, half Subtractor , full subtractor, Block diagram of parallel adder using full adder block (up to 4 - bit) 3.2 Encoder (4:2, 8:3) Decoder (2:4, 3:8) 3.3 Multiplexers (2:1, 4:1, 8:1) Demultiplexers (1:2, 1:4, 1:8) 3.4 Binary to Gray and Gray to binary code converters
Unit-IV **Sequential logic circuits**	4a. Describe the function of various types of flip-flops with the help of circuit diagram, truth table. 4b. Describe the working of shift Registers with the help of circuit diagram, truth table. 4c. Explain the working of various types of Counters with the help of circuit diagram, truth table.	4.1 Flip-flops: SR, D, JK, T, JK Master Slave, Triggering 4.2: Shift Registers: Classification of Shift Registers, Serial in serial-out, serial-in parallel-out, parallel-in serial-out and parallel-in parallel out. 4.3 Counters: Ring Counter, Johnson Counter, 4 bit Asynchronous (Ripple) Counter, 4 bit Synchronous up/down Counter, BCD/Decade counter.
Unit-V **Introduction to Memories and logic families**	5a. Classify semiconductor Memories 5b. Identify different types of Memories. 5c. Compare Logic families. 5d. Manage E-waste of Digital ICs/Chips	5.1 Introduction and Types of Memory: 5.1.1 RAM (SRAM, DRAM) 5.1.2 ROM (PROM, EPROM, EEPROM) 5.2 Overview of different logic family Definitions: Fan in, Fan out, Noise margin, Propagation delay, Power dissipation, Figure of merit 5.3 Comparison of different logic families (TTL, CMOS, ECL) 5.4 E-waste Management of Digital ICs/Chips

9. SUGGESTED SPECIFICATION TABLE FOR QUESTIONPAPER DESIGN

Unit No.	Unit Title	Teaching Hours	Distribution of Theory Marks			
			R Level	U Level	A Level	Total Marks
I	Number systems and codes	8	2	6	4	12
II	Boolean algebra and Logic gates	9	4	6	6	16
III	Combinational logic circuits	9	4	8	4	16
IV	Sequential logic circuits	9	4	8	4	16
V	Introduction to Memories and logic families	7	4	4	2	10
Total		**42**	**18**	**32**	**20**	**70**

Legends: *R=Remember, U=Understand, A=Apply and above (Revised Bloom's taxonomy)*

10. SUGGESTED STUDENT ACTIVITIES

Other than the classroom and laboratory learning, following are the suggested student-related ***co-curricular*** activities which can be undertaken to accelerate the attainment of the various outcomes in this course: Students should perform following activities in group and prepare reports of about 5 pages for each activity. They should also collect/record physical evidences for their (student's) portfolio which may be useful for their placement interviews:

I. Read and note down specifications of Digital ICs using data sheet: IC number/ Pin Diagram/voltage levels, applications for the following Digital ICs (TTL/CMOS): AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR gates, Decoder, Multiplexer, BCD to 7-segment decoder, SR FF,JK FF, D FF, shift Register, Counter, ADC, DAC.
ii. Solve real life problems using binary logic theory and implement it using digital logic circuits.
iii. Explore working of Digital clock/Digital panel.
iv. Prepare micro project using Various Digital IC and display devices.

11. SUGGESTED SPECIAL INSTRUCTIONAL STRATEGIES (if any)

These are sample strategies, which the teacher can use to accelerate the attainment of the various outcomes in this course:

a) Massive open online courses (***MOOCs***) may be used to teach various topics/sub topics.
b) Guide student(s) in undertaking micro-projects.
c) ***'L' in section No. 4*** means different types of teaching methods that are to be employed by teachers to develop the outcomes.
d) About ***20% of the topics/sub-topics*** which are relatively simpler or descriptive in nature is to be given to the students for ***self-learning***, but to be assessedusing different assessment methods.
e) With respect to ***section No.10***, teachers need to ensure to create opportunities and provisions for ***co-curricular activities***.
f) Introduce E-waste recycling technology among the students.

g) Internet based home assignments

h) Micro projects (in group of three to four students)

12. SUGGESTED MICRO-PROJECTS

Only one micro-project is planned to be undertaken by a student that needs to be assigned to him/her in the beginning of the semester. In the first four semesters, the micro-projects are group-based (group of 3 to 5). However, **in the fifth and sixth semesters**, the number of students in the group should ***not exceed three.***

The micro-project could be industry application based, internet-based, workshop-based, laboratory-based or field-based. Each micro-project should encompass two or more COs which are in fact, an integration of PrOs, UOs and ADOs. Each student will have to maintain dated work diary consisting of individual contribution in the project work and give a seminar presentation of it before submission. The duration of the micro project should be about **14-16** ***(fourteen to sixteen) student engagement hours*** during the course. The students ought to submit micro-project by the end of the semester to develop the industry-oriented COs.

A suggestive list of micro-projects is given here. This has to match the competency and the COs. Similar micro-projects could be added by the concerned course teacher:

a) Implement Logic Gates on General Purpose Board.

b) Implement simplified Product of Sum (POS) based equation using logic gates on General Purpose Board.

c) Design Half Adder/Full Adder Circuit on General Purpose Board.

d) Design Half Subtractor/Full Subtractor Circuit on General Purpose Board.

e) Design 4:1 Multiplexer on General Purpose Board.

f) Design 4 bit Gray to Binary code converter on General Purpose Board.

g) Design any Flip-flop on General Purpose Board.

h) Design 4-bit Counter on General Purpose Board.

i) Identify Various types of Memories like Pen Drive, Hard Disk, DVD, Memory Card etc. around you and Prepare a chart of it.

j) Identify E-Waste of Digital ICs and Prepare a brief Report of Remedies for it.

13. SUGGESTED LEARNING RESOURCES

Sr. No.	Title of Book	Author	Publication with place, year and ISBN
1	Digital Logic and Computer Design	M. Morris Mano	Pearson Education India; First edition (2016) ISBN-10 : 933254252X ISBN-13 : 978-9332542525

Sr. No.	Title of Book	Author	Publication with place, year and ISBN
2	Digital Principles and Application	Malvino and Leach	TMH Pub., New Delhi, 7th Edition or latest ISBN-10 : 0070141703 ISBN-13 : 978-0070141704
3	Fundamentals of Digital Circuits	A. Anand Kumar	PHI Learning, New Delhi, 4th Edition ISBN-10 : 8120352688 ISBN-13 : 978-8120352681
4	Modern Digital Electronics	Jain, R P	TMH Education , New Delhi, 4th Edition ISBN-10 : 0070669112 ISBN-13 : 978-0070669116
5	Digital Electronics	Kharate G.K.	OXFORD University Press, 2012 ISBN-10: 0198061838 ISBN-13: 9780198061830
6	Digital Electronics	B.R. Gupta V. Singhal	S K Kataria and Sons (2012) ISBN-10: 9380027885 ISBN-13: 978-8185749600
7	A Textbook of Digital Electronics	S. S. Bhatti Rahul Malhotra	I K International Publishing House Pvt. Ltd (2011) ISBN-10 : 9381141517 ISBN-13 : 978-9381141519

14. SOFTWARE/LEARNING WEBSITES

- https://nptel.ac.in/courses/117/106/117106086/
- https://www.tutorialspoint.com/digital_circuits/index.htm
- https://www.javatpoint.com/digital-electronics
- https://www.javatpoint.com/combinational-logic-circuits-in-digital-electronics (for combinational logic circuits)
- https://www.electronicsforu.com/technology-trends/learn-electronics/flip-flop-rs-jk-t-d (for flip-flops)
- https://www.javatpoint.com/shift-registers-in-digital-electronics (for shift registers)
- https://www.javatpoint.com/counters-in-digital-electronics (for counters)
- https://www.mphysicstutorial.com/2020/12/semiconductor-memory-types-ram-rom-dram.html (for semiconductor memories)
- https://www.electrically4u.com/classification-and-characteristics-of-digital-logic-family/
- https://de-iitr.vlabs.ac.in/ (Virtual Labs for experiments)
- http://vlabs.iitkgp.ernet.in/dec/ (Virtual Labs for experiments)

- Logisim: (educational tool for designing and simulating *digital logic* circuits) available at: https://sourceforge.net/projects/circuit/ (Digital Circuit simulation open source software)

15. PO-COMPETENCY-CO MAPPING

Semester II	Digital Electronics (Course Code: 4321103)						
	POs						
Competency & Course Outcomes	**PO 1 Basic & Discipline specific knowledge**	**PO 2 Problem Analysis**	**PO 3 Design/ develop-ment of solutions**	**PO 4 Engineering Tools, Experimen-tation&Testing**	**PO 5 Engineering practices for society, sustainability & environment**	**PO 6 Project Manage-ment**	**PO 7 Life-long learning**
Competency	**Maintain the digital electronic circuits.**						
Course Outcomes CO 1) Interpret various number systems and their conversions with binary arithmetic operations.	3	1	1	1	-	1	1
CO 2) Implement simplified Boolean equations using logic gates.	3	3	2	2	-	2	1
CO 3) Test different types of combinational logic circuits.	3	2	2	2	-	2	1
CO 4) Test different types of sequential logic circuits.	3	2	2	2	-	2	1
CO 5) Classify various memories and logic families.	3	1	2	2	2	2	2

*Legend: '**3**' for high, '**2**' for medium, '**1**' for low and '**-**' for no correlation of each CO with PO.*

16. COURSE CURRICULUM DEVELOPMENT COMMITTEE

GTU Resource Persons

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